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Paper Code : PC-EE 402/PC-EEE 402 Digital Electronic

UPID : 004419

Time Allotted : 3 Hours

Full Marks : 70

The Figures in the margin indicate full marks.

Candidate are required to give their answers in their own words as far as practicable

Group-A (Very Short Answer Type Question)

1. Answer any ten of the following :

[1 x 10 = 10]

- (I) What is the difference between digital signal and discrete signal?
- (II) In a DRAM, what is the state of R/W during a read operation?
- (III) A binary-weighted digital-to-analog converter has an input resistor of 100 k Ω . If the resistor is connected to a 5 V source, the current through the resistor is:
- (IV) What is the meaning of RAM, and what is its primary role?
- (V) How is an encoder different from a decoder?
- (VI) How you can convert a two-input NAND gate to an inverter?
- (VII) The difference between analog voltage represented by two adjacent digital codes, or the analog step size, is known as _____.
- (VIII) A 64-bit word consists of _____.
- (IX) Convert the following SOP expression to an equivalent POS expression.
 $A B C + A \bar{B} \bar{C} + A \bar{B} C + A B \bar{C} + \bar{A} \bar{B} C$
- (X) If two inputs are active on a priority encoder, which will be coded on the output?
- (XI) From the truth table below, determine the standard SOP expression.

Inputs			Output
A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

- (XII) What is difference between Frequency Division multiplexing and Wave Division multiplexing?

Group-B (Short Answer Type Question)

Answer any three of the following :

[5 x 3 = 15]

2. What is a multiplexer circuit? Briefly describe one or two applications of a multiplexer? [5]
3. What is meant by the race around problem in J-K flip-flops? How does a master–slave configuration help in solving this problem? [5]
4. Design the circuit by following proper steps for the Boolean expressions of the two output variables given in the equations below. [5]

$$D = \bar{A}.\bar{B}.B_{in} + \bar{A}.B.\bar{B}_{in} + A.\bar{B}.\bar{B}_{in} + A.B.B_{in}$$

$$B_o = \bar{A}.\bar{B}.B_{in} + \bar{A}.B.\bar{B}_{in} + \bar{A}.B.B_{in} + A.B.B_{in}$$
5. What is a flip-flop? Show the logic implementation of an R-S flip-flop having active HIGH R and S inputs. Draw its truth table and mark the invalid entry. [5]
6. Starting with the Boolean expression for a two-input OR gate, apply Boolean laws and theorems to modify it in such a way as to facilitate the implementation of a two-input OR gate by using two-input NAND gates only. [5]

Group-C (Long Answer Type Question)

Answer any three of the following :

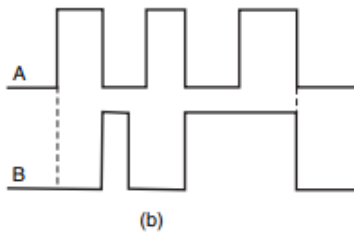
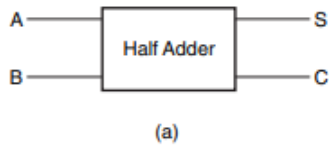
[15 x 3 = 45]

7. What is meant by the radix or base of a number system? Briefly describe why hex representation is used for the addresses and the contents of the memory locations in the main memory of a computer. Assume a radix-32 arbitrary number system with 0–9 and A–V as its basic digits. Express the mixed binary number $(110101.001)_2$ in this arbitrary number system. [5+10]

8. (a) How do you characterize or define a combinational circuit? How does it differ from a sequential circuit? Give two examples each of combinational and sequential logic devices. [7]

- (b) For the half-adder circuit of following figure, the inputs applied at A and B are as shown in graphical form. [8]

Plot the corresponding SUM and CARRY outputs on the same scale.



9. (a) How do you distinguish between positive and negative logic systems? Prove that an OR gate in a positive logic system is an AND gate in a negative logic system. [7]

- (b) Why are NAND and NOR gates called universal gates? Justify your answer with the help of examples. [4]

- (c) What are logic gates with open collector or open drain outputs? What are the major advantages of such devices? [4]

10. (a) Implement the product-of-sums Boolean function expressed by $\Sigma(0,3,4,6,7)$ by a suitable multiplexer. [8]

- (b) What is a demultiplexer and how does it differ from a decoder? Can a decoder be used as a demultiplexer? If yes, from where do we get the required input line? [7]

11. (a) A certain eight-bit D/A converter has a full-scale output of 5 mA and a full-scale error of $\pm 0.25\%$ of full scale. Determine the range of expected analogue output for a digital input of 10000010. [8]

- (b) The data sheet of a certain eight-bit A/D converter lists the following specifications: resolution eight bits; full-scale error 0.02 % of full scale; full-scale analogue input +5 V. Determine (a) the quantization error (in volts) and (b) the total possible error (in volts). [7]

*** END OF PAPER ***